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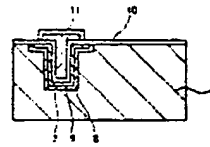
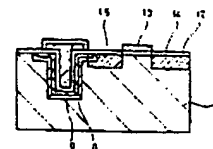
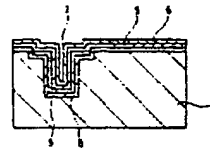
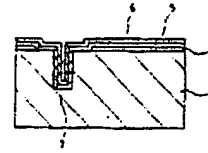
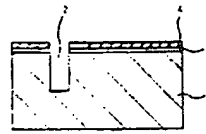
APPLICATION DATE : 18-10-85
APPLICATION NUMBER : 60233828

APPLICANT : SANYO ELECTRIC CO LTD;

INVENTOR : AKAISHI YOSHIO;

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TITLE : FORMING METHOD FOR CAPACITY
OF SEMICONDUCTOR MEMORY CELL



ABSTRACT : PURPOSE: To readily obtain an Hi-C structure by superposing and bonding the first glass layer containing a P-type impurity and the second glass layer containing an N-type impurity on the side of a groove, and simultaneously diffusing to form the P-type first diffused regions and the N-type second diffused region.

CONSTITUTION: A P-type silicon semiconductor substrate 1 is covered with a silicon oxide film 3 and a CVD silicon nitride film 4, the substrate 1 formed with the prescribed groove 2 is exposed, anisotropically etched by RIE to form the groove 2. The first glass layer 5 containing a P-type impurity and the second glass layer 6 containing an N-type impurity are laminated on the substrate 1 including the side of the groove 2. The layers 5, 6 are bonded to the sides of the groove 22 and the substrate 1 of the periphery of the groove 2, and the other portion of the substrate 1 is covered with a silicon oxide film 7. P-type and N-type impurities are simultaneously diffused in the side of the groove 2 to form the first and second diffused regions 8, 9. Then, a thin insulating film 10 is formed on the groove 2, and a cell-plate electrode 11 is formed on the film 10.

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